

## Optimal design of three-phase solar PV integrated unified power quality conditioner (UPQC)

Yogesh S. Pawar<sup>1</sup>, Mahesh Kadu<sup>2</sup>, Pawan C. Tapre<sup>3</sup>, Dinesh S. Wankhede<sup>4</sup>, Rajendra M. Rewatkar<sup>5</sup>, Swapna M. Choudhary<sup>6</sup>, Rakesh G. Shriwastava<sup>7</sup>

<sup>1</sup>Department of Electrical Engineering, Loknete Gopinathaji Munde Institute of Engineering Education and Research, Nashik, India

<sup>2</sup>Department of Electronics and Telecommunications Engineering, Amrutvahini College of Engineering, Sangamner, India

<sup>3</sup>Department of Electrical Engineering, S.N.D. College of Engineering and Research Center, Nashik, India

<sup>4</sup>Department of Electrical Engineering, St. Vincent Pallotti College of Engineering and Technology, Nagpur, India

<sup>5</sup>Department of Artificial Intelligence and Data Science, Faculty of Engineering and Technology,

Datta Meghe Institute of Higher Education and Research, Wardha, India

<sup>6</sup>Department of Electronics and Telecommunications Engineering, GH Raison College of Engineering, Nagpur, India

<sup>7</sup>Department of Electrical Engineering, Govindrao Wanjari College of Engineering and Technology, Nagpur, India

### Article Info

#### Article history:

Received Apr 1, 2024

Revised Jun 28, 2025

Accepted Aug 3, 2025

#### Keywords:

Compensator UPQC

MPPT

Power quality

Shunt compensator series

Solar PV

### ABSTRACT

This research investigates the utilization of a unified power quality conditioner (UPQC) to address power quality issues in the electrical grid and mitigate harmonics introduced by non-linear loads. The UPQC system is augmented by a combination of photovoltaic (PV) and battery energy storage system (BESS). Typically, the PV system supplies active power to the load. However, in cases where the PV system cannot provide sufficient power, the BESS is activated to ensure a continuous power supply, particularly during prolonged voltage interruptions. To enhance system reliability and reduce dependency on environmental conditions, a hybrid PV-BESS system is proposed. The inclusion of the BESS improves long-term voltage support capabilities, simplifies the DC-link voltage regulation algorithm, and facilitates the production of clean energy. For efficient phase synchronization operation of the UPQC controller under unbalanced and distorted grid voltage conditions, a self-tuning filter (STF) integrated with the unit vector generator (UVG) technique is employed.

This is an open access article under the [CC BY-SA](#) license.



### Corresponding Author:

Yogesh S. Pawar

Department of Electrical Engineering

Loknete Gopinathaji Munde Institute of Engineering Education and Research

Nashik, Maharashtra 422002, India

Email: [yogesh.pawar@logmicer.edu.in](mailto:yogesh.pawar@logmicer.edu.in)

## 1. INTRODUCTION

The concept of flexible AC transmission systems (FACTS) involves the application of advanced power electronics technology to existing AC transmission systems [1], [2]. This technology aims to enhance stability and increase the usable power transmission capacity up to its thermal limit. One of the devices used in FACTS is the unified power quality conditioner (UPQC), which provides simultaneous control over transmission line impedance, phase angle, and voltage [3]-[5]. The UPQC consists of two power electronic inverters that are interconnected via a shared DC link. These inverters are accompanied by transformers, which serve the purpose of isolating the UPQC and aligning the voltage levels between the power system and the power electronic inverters [6]-[8]. One of the inverters is directly connected to the transmission line and serves as a series inverter. It has the ability to generate a controllable voltage with adjustable magnitude and phase angle. This series inverter is capable of supplying both real and reactive power to the transmission line,

thus offering control over power flow. The second inverter is primarily responsible for supplying the real power required by the series inverter but can also function independently as a VAR compensator. This arrangement allows the UPQC to effectively manage the flow of both real and reactive power within the transmission line [8]-[10].

The UPQC comprises two voltage source inverters (VSIs) that can operate autonomously by isolating the DC side. When configured in this manner, the shunt inverter performs as a static synchronous compensator (STATCOM) [11]-[14]. Its main role is to generate or absorb reactive power in order to regulate the voltage magnitude at the point of connection. On the other hand, the series inverter functions as a static synchronous series compensator (SSSC). It is responsible for generating or absorbing reactive power to control the current flow and subsequently regulate the power flow on the transmission line [15]-[18]. This arrangement ensures that the voltage and power characteristics of the system are effectively managed while addressing power quality issues. The UPQC offers the advantage of separately controlling real and reactive power, making it suitable for improving power quality. In this proposed study, a two-bus system is modeled and simulated with the inclusion of UPQC. Additionally, a 14-bus system is modeled and simulated with and without UPQC. The investigation of real and reactive power reveals that the real power increases with the injection angle, while the reactive power increases with the shunt voltage injection [19]-[25].

Simulink models are developed for three types of UPQC: pulse width modulation (PWM) inverter-based UPQC, space vector modulation (SVM) inverter-based UPQC, and multilevel inverter (MLI)-based UPQC. The results from these three cases are compared. Furthermore, the concept of multiple and distributed dynamic voltage restorer (DVR) is introduced to enhance the voltage profile of the system. This paper is organized as follows: section 1 describes the introduction, section 2 describes the methodology, section 3 presents the results and discussions, and section 4 provides the conclusion.

## 2. METHODOLOGY

The above literature does not deal with modeling 14 and 30-bus systems using MATLAB/Simulink. This work proposes models for 14 and 30-bus systems employing UPQC. The effects on real power and reactive power and voltage are investigated. This work deals with the control of real and reactive power in power system using MATLAB/Simulink. A unified power flow controller (UPQC) is a shunt-series type converter used for improving power quality. The UPQC controls the real and reactive powers by varying the firing angle of the rectifier and inverter. The circuit model for UPQC is developed using MATLAB/Simulink and it is used for simulation studies for various systems. Multilevel inverter-based UPQC is not present in the literature. SVM-based UPQC system does not exist in the literature. This work proposes SVM-based UPQC system and multilevel inverter for the control of power. The concept of UPQC with distributed DVR is proposed to improve the voltage quality.

### 2.1. Literature survey

Kim and Sul [1] discussed the control of compensation voltages in dynamic voltage restorers (DVRs). They analyzed the power circuit of a DVR system to establish control limitations and targets for compensation voltage control. They developed a combined feedforward and state feedback control structure for the compensation voltages, considering control delay and closed-loop damping factor. Gao *et al.* [2] analyzed Z-source inverter modulation and demonstrated how conventional PWM strategies for voltage source inverters can be modified for Z-source inverters. They verified their theoretical and modulation concepts through simulations and experiments.

Vilathgamuwa *et al.* [3] proposed a new topology based on the Z-source inverter for DVRs to enhance voltage restoration. The proposed topology utilized the shoot-through capability of the inverter to ensure a constant DC voltage across the DC link, improving energy utilization. The system and its controller were tested through simulations and experiments, demonstrating effective compensation of voltage sags while fully utilizing stored energy. Ramasamy *et al.* [4] presented a DVR system using three-dimensional space vector pulse width modulation (3D-SVPWM). Their control scheme mitigated zero sequence components by including a zero-axis in addition to the conventional alpha-beta axes. The proposed solution offered versatile voltage sag compensation for fault-affected three-phase power systems.

Omar and Rahim [5] discussed DVR control based on d-q transformation. They presented a control system that utilized a scaled error of the DVR's source side and its reference for sag/swell correction. The DVR provided quick compensation, excellent voltage regulation, and could handle balanced and unbalanced situations effectively. Lam *et al.* [6] addressed voltage swell and overvoltage compensation in a diode bridge rectifier-supported transformer-less coupled DVR. They proposed a novel unidirectional power flow control algorithm that effectively suppressed the continuous rise in the DC link voltage during swells. Simulation and experimental results for unbalanced voltage swell compensation were presented.

Benachaiba and Ferdi [7] discussed DVR principles and voltage restoration methods at the point of common coupling. They highlighted the effectiveness and efficiency of DVRs in solving voltage sag and swell problems, emphasizing their lower cost, smaller size, and fast dynamic response. Nour and Helal [8] presented a DVR based on a firing control strategy for a three six-switch voltage source inverter (VSI). Their strategy combined 180 and 120 conduction modes to generate a new operating mode, resulting in a seven-level, 12-step output voltage waveform resembling a sinusoidal shape.

Naidu [9] described the closed-loop control of a four-leg voltage source converter (VSC)-based DVR. They used a weighted, recursive, least square estimator to resolve the three-phase input variables into positive, negative, and zero sequence components. They tested the performance of the DVR through simulations and experiments. Kumar and Mishra [10] proposed a filter structure to improve the performance of a switching band controller-based DVR. They presented the filter structure and an adaptive band controller for the DVR, highlighting the fast dynamic response, robustness, and ease of implementation. The proposed approach was validated through power systems computer aided design (PSCAD) simulation studies.

## 2.2. Basic circuit of UPQC

The unified power flow controller (UPQC) is composed of two switching converters, specifically voltage-source inverters, as depicted in Figure 1. These inverters, referred to as "Converter 1" and "Converter 2" are shown in Figure 1 and operate using a shared DC link provided by a DC storage capacitor. This configuration functions as an ideal AC-to-AC power converter, allowing real power to flow bidirectionally between the AC terminals of the two inverters. Each inverter can independently generate or absorb reactive power at its respective AC output terminal. Figure 1 shows UPQC connected to a transmission line.

## 2.3. Control strategy for shunt converter

The measured load current is converted into a synchronous duo-reference system. With this transformation, the underlying positive-sequence components converted to d- and q-axis DC amplitudes can be easily extracted by a low-pass filter (LPF). Furthermore, all harmonic components are transformed into AC quantities with a fundamental frequency shift [3].

The shunt compensator operates at maximum power and draws maximum power from the PV system. The maximum power point tracking (MPPT) algorithm creates a DC link voltage reference for UPQC. Current from the intermediate circuit is transferred to the network by electricity. The mains current is compared with the target current and fed to the hysteresis controller. A hysteresis controller generates the gate pulse for the shunt converter [8]. Figure 2 deals with the control structure of the shunt compensator.

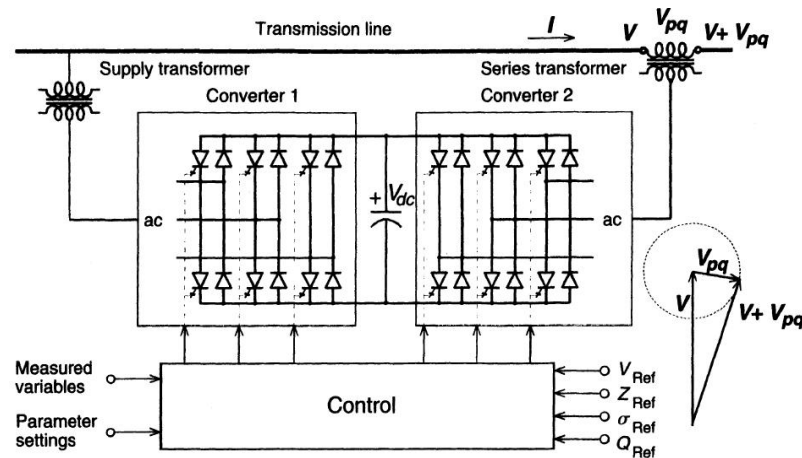


Figure 1. UPQC connected to a transmission line

## 2.4. Control of series compensator

The bus voltage is sensed and converted to a synchronous dq0 reference frame. Series compensator control strategies include pre-embedded compensation, common-mode compensation, and power-optimized compensation. In this study, the series compensator applies a voltage that is in phase with the supply voltage, which helps to produce the minimum voltage applied to the series compensator. Figure 3 shows the control structure of the series compensator. The base component of the PCC voltage was extracted using the PLL and used to generate reference axes in the d-q-0 domain. The reference load voltage is generated using phase and frequency detection of the PCC voltage obtained with the PLL.

The PCC voltage and the load voltage are transformed into the d-q-0 domain. The load reference voltage must be in phase with the PCC voltage, so the peak load reference voltage is the value of the d-axis component of the load reference voltage. The q-axis component is kept at zero. The change between the load reference voltage and the PCC voltage produces the reference voltage for the series compensator. The change between the load voltage and the PCC voltage produces the actual series compensator voltage. The change between the reference voltage and the actual series compensator voltage is fed to the PI controller to generate the appropriate reference signal. These signals are converted to the ABC domain and fed through a pulse width modulation (PWM) voltage regulator to generate a suitable gate signal for the series compensator [15]. Figure 3 shows the control structure of the series compensator.

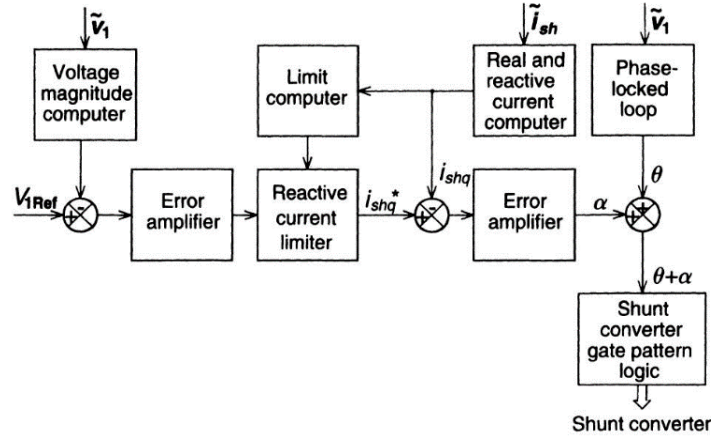


Figure 2. Control structure of shunt compensator

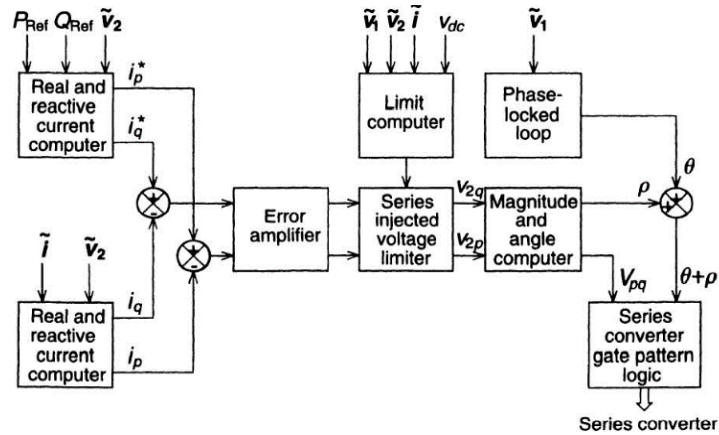


Figure 3. Control structure of series compensator

### 3. RESULTS AND DISCUSSION

The three-phase system is designed for the PV-BESS-UPQC model. The PV-BESS-UPQC comprises of series and shunt APF compensator linked with DC-link split capacitor. The battery and the PV array are linked parallelly to the DC-link. The PV is linked through a boost converter to the DC-link. Moreover, the BESS is linked through a buck-boost converter to the DC-link. The series compensator works like a controlled voltage source manner and mitigates the supply voltage sags, swells, interruptions, and voltage harmonic. On the other hand, the shunt compensator mitigates the current harmonics for the load. Both the series and shunt APF compensator are attached through interfacing inductors. In the UPQC system configuration, due to the converter switching action, harmonics are generated and therefore, a ripple filter is utilized to filter out harmonics. The series compensator uses a series injection transformer to insert voltage to the grid. In this work, a three-phase non-linear load is utilized. The PV-BESS-UPQC design procedure starts with the accurate measurement of PV array, split capacitor, and reference voltage of DC-link. The design of

the shunt compensator follows the way that apart from mitigating current harmonics it controls the peak output power from PV array. Figure 4 shows MATLAB simulation for three phase inverter integrated FC. Figure 5 shows three-phase grid voltage and current for integrated UPQC. Figure 6 shows three phase shunt inverter voltage and shunt inverter current for integrated UPQC. Figure 7 shows comparison between grid voltage, load voltage, and voltage injection for integrated UPQC. Figure 8 shows load voltage and load current before the inveter integrated UPQC. Figure 9 shows power-voltage curve of PV system for different irradiance and power-current curve of PV system for different irradiance.

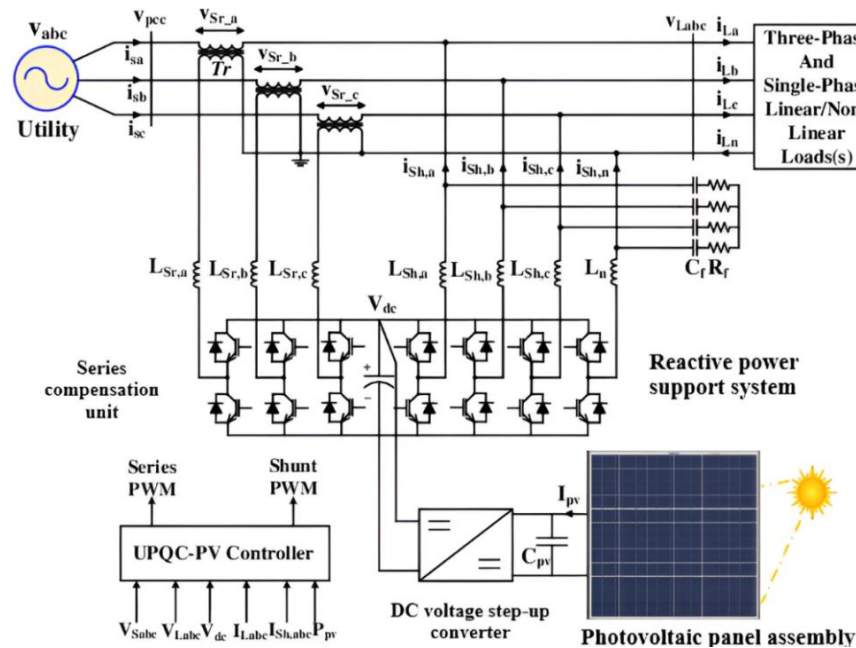


Figure 4. MATLAB simulation for three phase inverter integrated FC

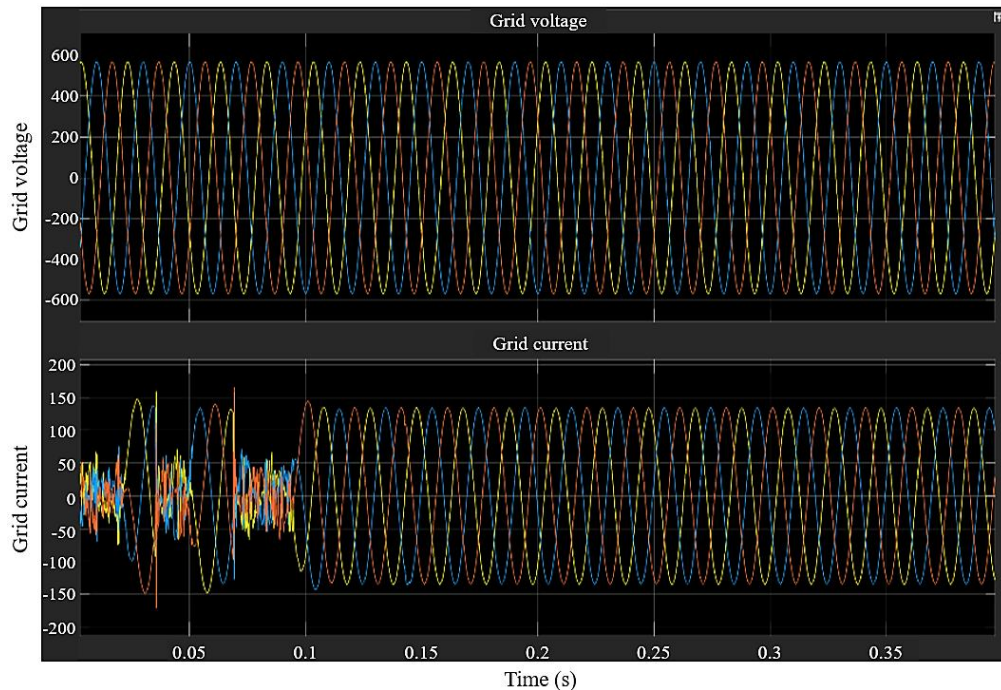


Figure 5. Three-phase grid voltage and current for integrated UPQC



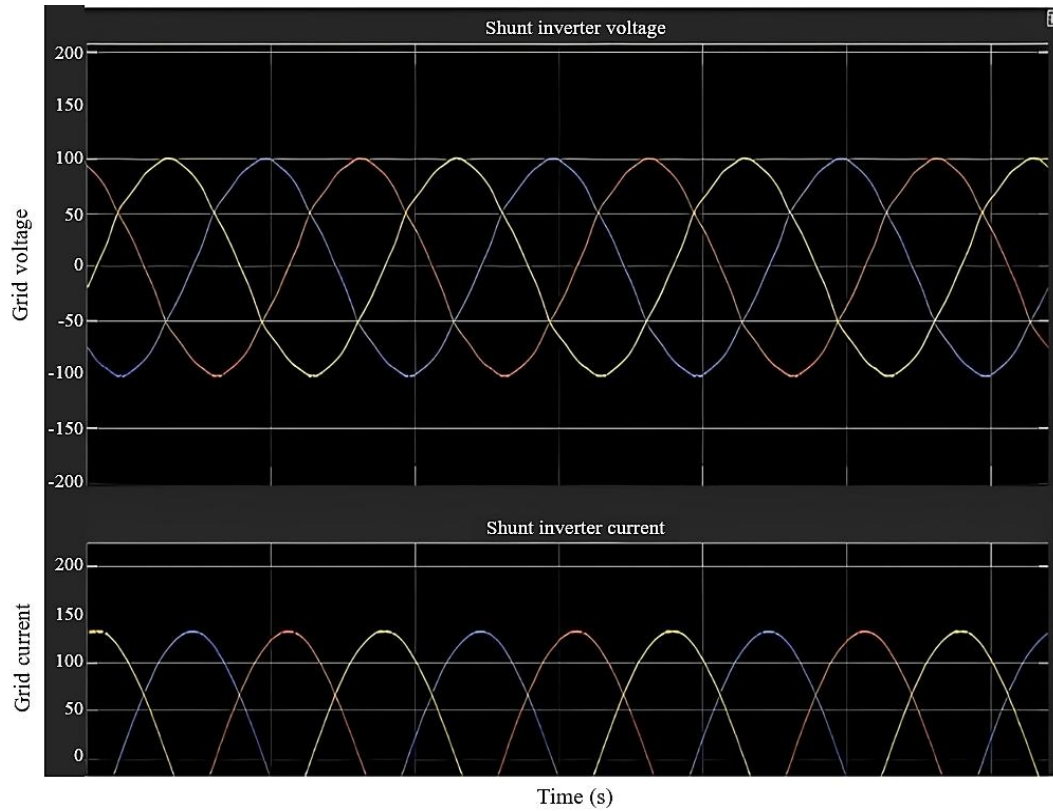


Figure 6. Three-phase shunt inverter voltage and shunt inverter current for integrated UPQC

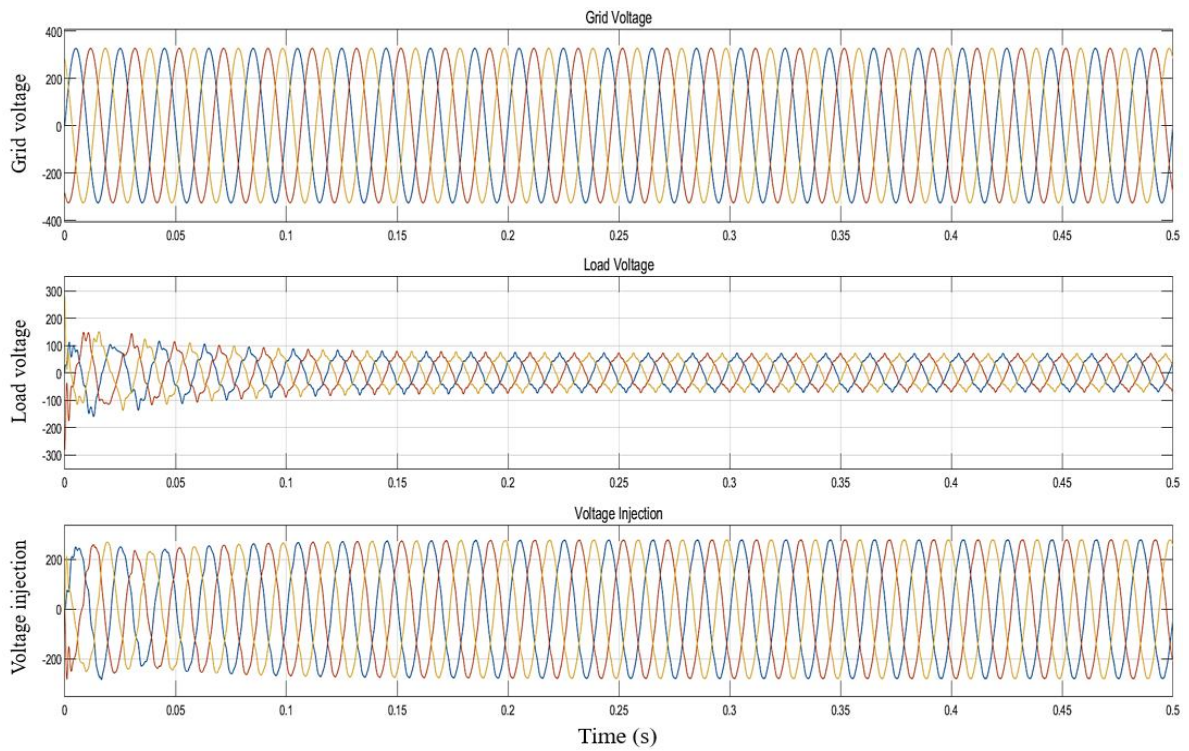


Figure 7. Comparison between grid voltages, load voltage, and voltage injection for integrated UPQC

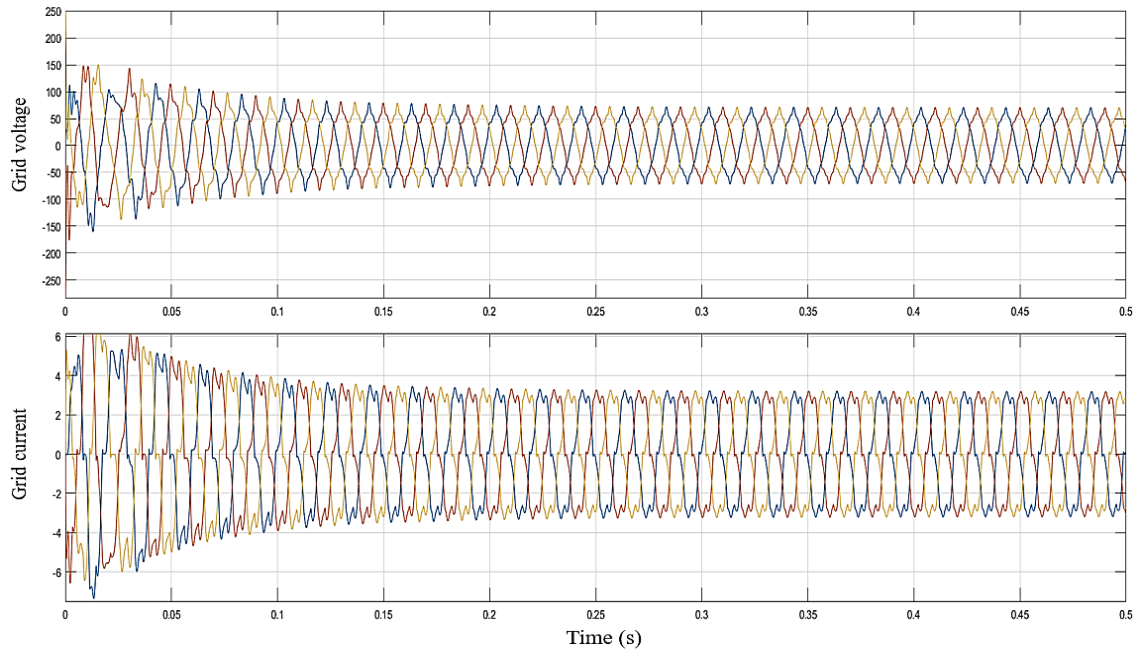


Figure 8. Load voltage and load current before the inverter integrated UPQC

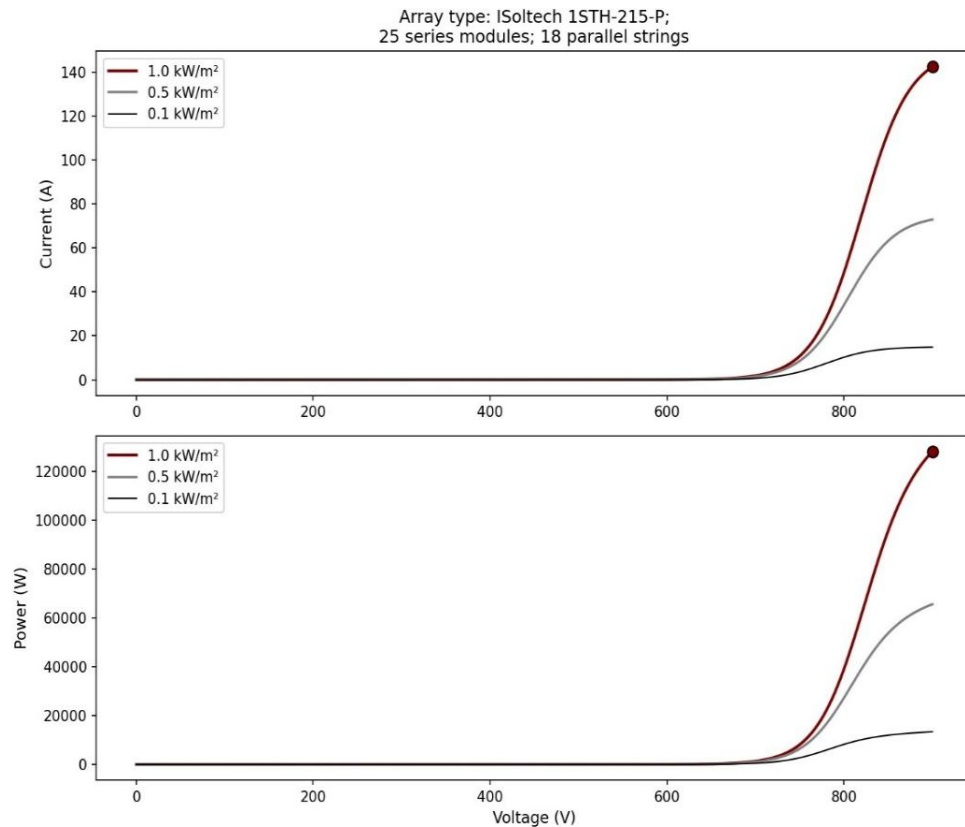


Figure 9. Power-voltage curve of PV system for different irradiance and power-current curve of PV system for different irradiance

The power vs voltage curve for a photovoltaic (PV) array describes the relationship between the output power and the operating voltage of the array. It provides valuable information about the array's performance under different conditions. The power vs voltage curve typically exhibits a characteristic shape known as the "I-V curve" (current vs voltage curve). The shape of the power vs voltage curve depends on

various factors, including the PV module technology, temperature, shading, and the amount of sunlight hitting the array. It is typically a downward-sloping curve, with the maximum power point located at a specific voltage and current combination. By analyzing the power vs voltage curve, engineers and system designers can optimize the operation of the PV array, ensuring it operates at or near the maximum power point for maximum energy conversion efficiency. Figure 10 illustrates the PV system output with respect to temperature, followed by the overall PV power output depicted in Figure 11. The corresponding load demand is presented in Figure 12, while the grid power profile is shown in Figure 13. Finally, Figure 14 displays the inverter power.

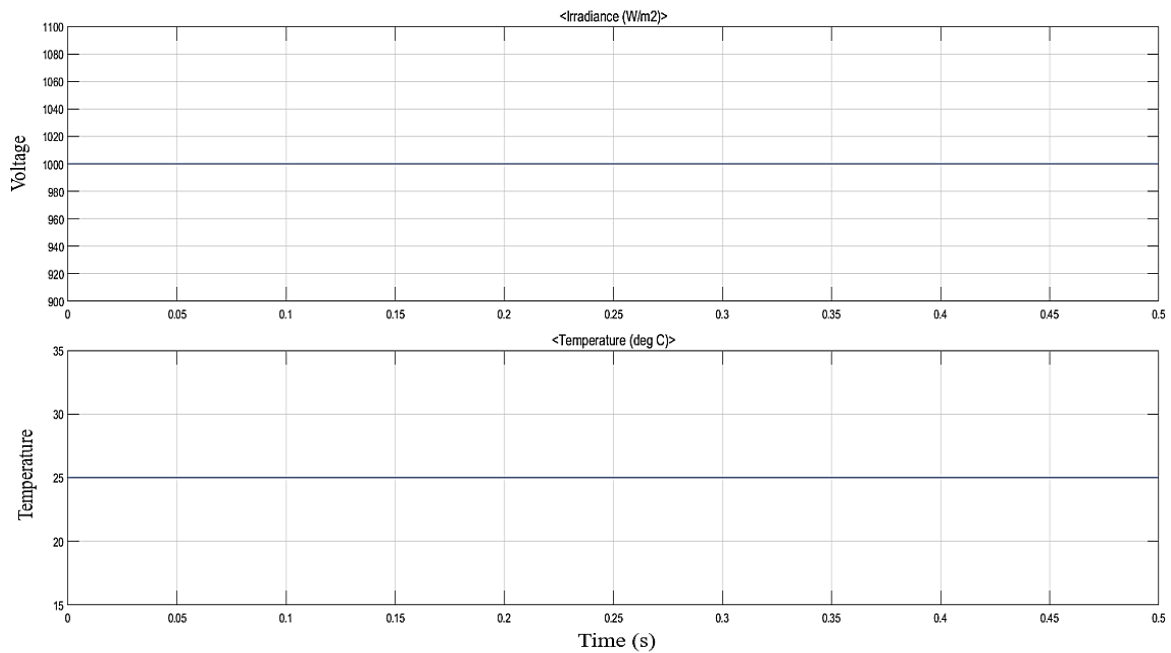


Figure 10. PV system output (temperature)

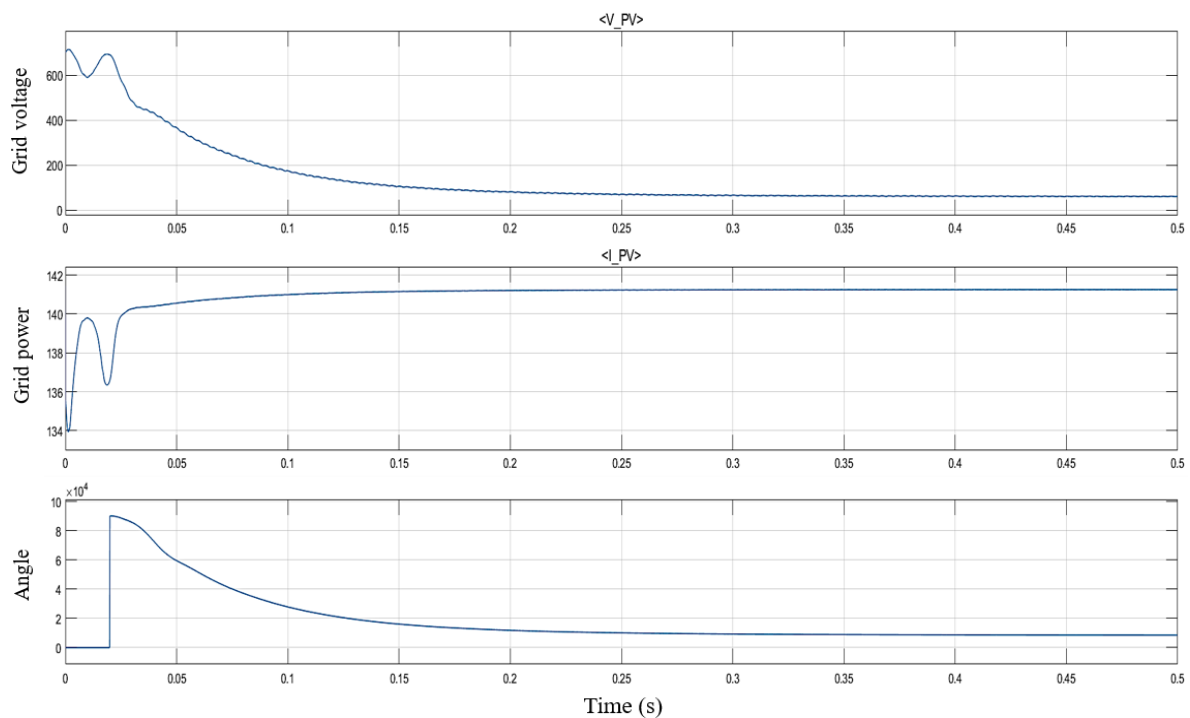


Figure 11. PV system output ( $P_{pv}$ ,  $I_{pv}$ ,  $V_{pv}$ )



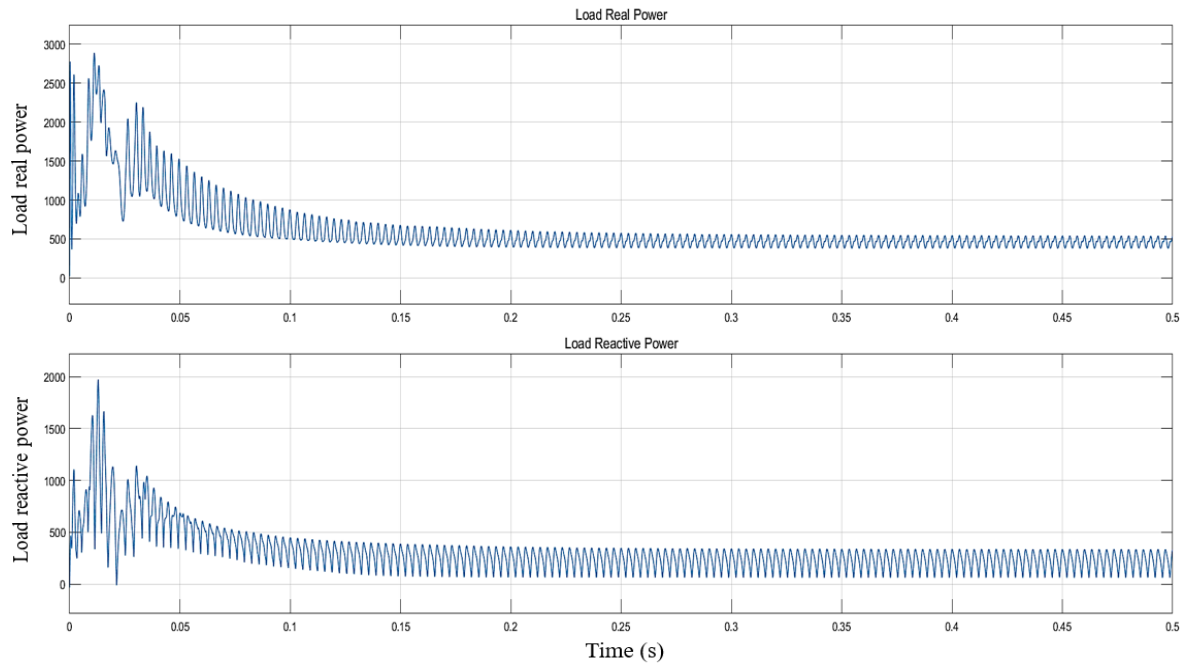


Figure 12. Load power

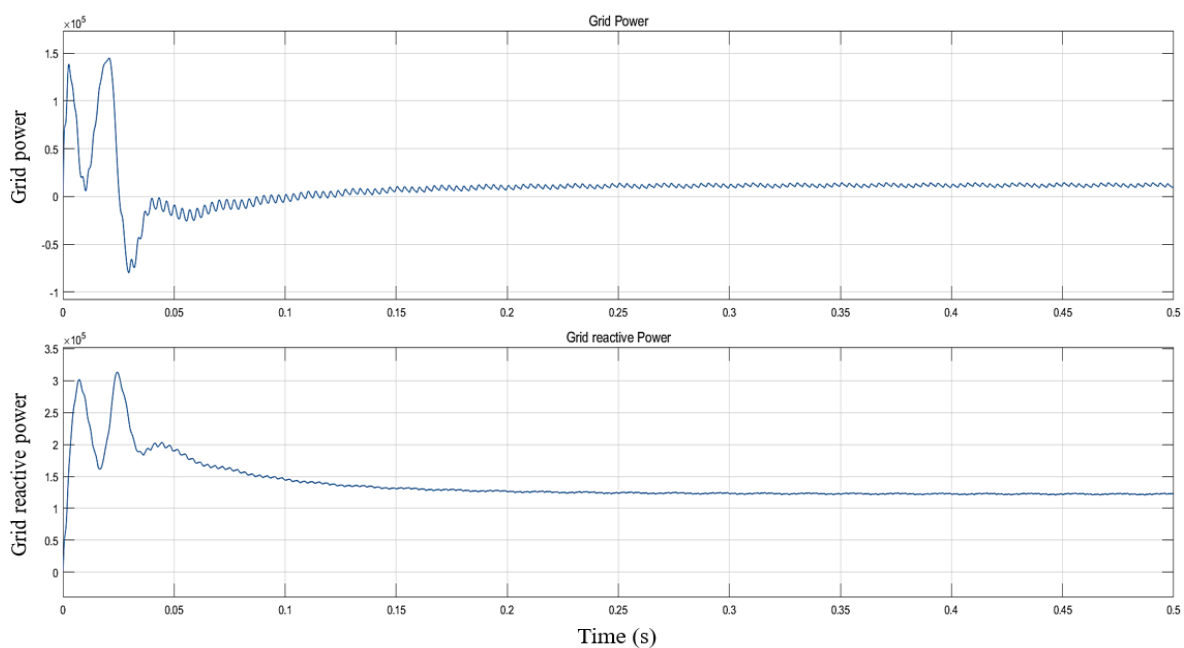


Figure 13. Grid power

The performance of a PV array is influenced by the environmental conditions, primarily temperature and irradiance (amount of sunlight). Here's a description of how these factors affect the PV array:

- Temperature:** The temperature of the PV array affects the efficiency and power output of the solar cells. Generally, as the temperature increases, the efficiency of the solar cells decreases. This is because higher temperatures can cause an increase in the internal resistance of the cells and reduce the voltage output. However, the decrease in efficiency varies depending on the specific technology and design of the PV modules.
- Irradiance:** The amount of sunlight or irradiance directly impacts the power output of the PV array. Higher levels of irradiance result in increased power generation, while lower levels of irradiance lead to reduced power output. PV arrays typically have a linear relationship between irradiance and power output, meaning that doubling the irradiance will roughly double the power output.

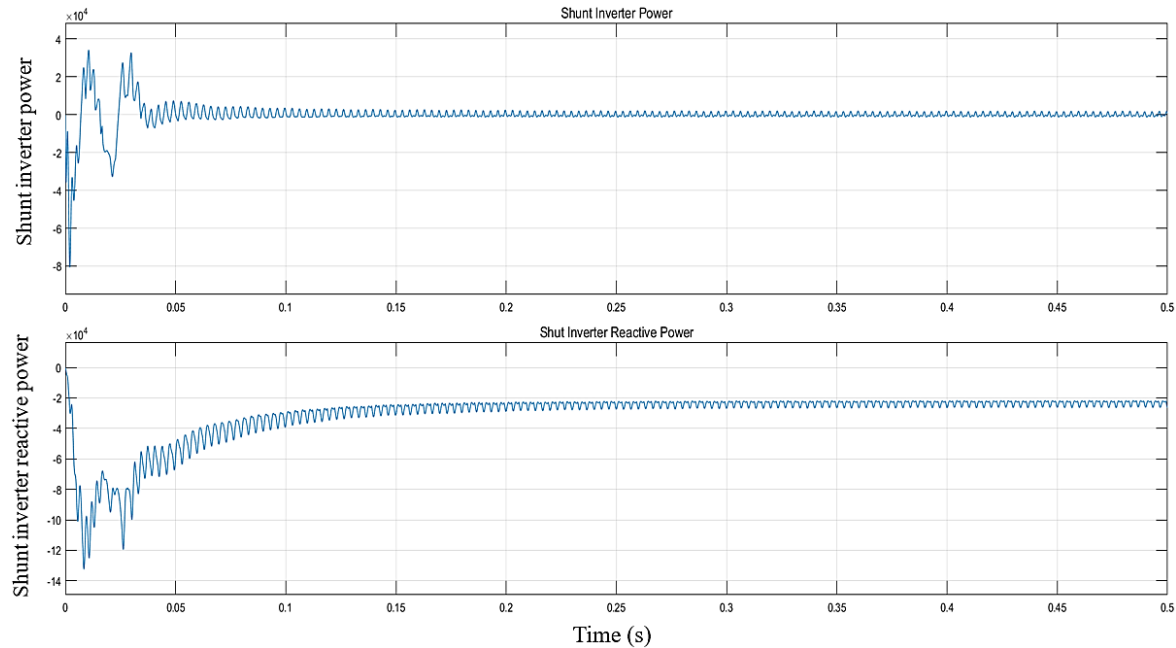


Figure 14. Inverter power

The results presented are studied on a single machine infinite bus (SMIB) power network, which reflects suitability of this approach in tuning UPQC control parameters and is also extendable to multi-area systems. In this model, two voltage sources are used to represent the fundamental components of the PWM-controlled output voltage waveform of the two branches in the UPQC. The impedance of the two coupling transformers is included in the proposed model, and the losses of UPQC depict the voltage source equivalent circuit of UPQC. The series injection branches a series injection voltage source and performs the main functions of controlling power flow, whilst the shunt branch is used to provide real power demanded by the series branch and the losses in the UPQC. However, in the proposed model, the function of reactive compensation of the shunt branch is completely neglected.

#### 4. CONCLUSION

This research paper introduces the new capabilities of performance investigation of optimal design three-phase solar PV integrated unified power quality conditioner (UPQC) as a hybrid renewable energy device with energy management techniques. The simulation results show the efficiency of the power angle control and the efficiency of the distribution equipment filtering device during the entire UPQC reduction test. This approach also ensures a constant/required low voltage of high quality. This document shows how to easily tune serial and parallel APFs without losing the ability to improve power quality and eliminate persistent currents. This scheme shows that a small index of the operating level reduces the maximum value of vibration associated with the current position and the effective forces drawn from that position, and responds to APF. It should be noted that the research results show potential future applications in renewable energy sources and smart grids.

#### FUNDING INFORMATION

Authors state no funding involved.

#### AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

| Name of Author        | C | M | So | Va | Fo | I | R | D | O | E | Vi | Su | P | Fu |
|-----------------------|---|---|----|----|----|---|---|---|---|---|----|----|---|----|
| Yogesh S. Pawar       | ✓ | ✓ | ✓  | ✓  | ✓  | ✓ |   | ✓ | ✓ | ✓ |    |    | ✓ |    |
| Mahesh Kadu           |   | ✓ |    |    |    | ✓ |   | ✓ | ✓ | ✓ | ✓  | ✓  |   |    |
| Pawan C. Tapre        | ✓ |   | ✓  | ✓  | ✓  | ✓ | ✓ |   | ✓ | ✓ | ✓  |    | ✓ | ✓  |
| Dinesh S. Wankhede    | ✓ |   |    |    | ✓  | ✓ |   |   | ✓ | ✓ |    |    |   |    |
| Rajendra M. Rewatkar  |   |   |    |    | ✓  |   | ✓ |   | ✓ | ✓ |    | ✓  |   | ✓  |
| Swapna M. Choudhary   |   | ✓ |    |    | ✓  |   |   |   | ✓ | ✓ |    |    |   |    |
| Rakesh G. Shriwastava | ✓ |   |    |    | ✓  |   |   |   | ✓ | ✓ |    |    |   |    |

C : Conceptualization

M : Methodology

So : Software

Va : Validation

Fo : Formal analysis

I : Investigation

R : Resources

D : Data Curation

O : Writing - Original Draft

E : Writing - Review &amp; Editing

Vi : Visualization

Su : Supervision

P : Project administration

Fu : Funding acquisition

## CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

## DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

## REFERENCES

- [1] H. Kim and S.-K. Sul, "Compensation voltage control in dynamic voltage restorers by use of feed forward and state feedback scheme," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1169–1177, Sep. 2005, doi: 10.1109/TPEL.2005.854052.
- [2] F. Gao, P. C. Loh, F. Blaabjerg, and C. J. Gajanayake, "Operational analysis and comparative evaluation of embedded Z-source inverters," in *2008 IEEE Power Electronics Specialists Conference*, IEEE, Jun. 2008, pp. 2757–2763, doi: 10.1109/PESC.2008.4592362.
- [3] D. M. Vilathgamuwa, P. C. Loh, and Y. Li, "Protection of microgrids during utility voltage sags," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1427–1436, Oct. 2006, doi: 10.1109/TIE.2006.882006.
- [4] A. Ramasamy, V. K. Ramachandaramurthy, R. K. Iyer, and L. Z. Liu, "Control of dynamic voltage restorer using TMS320F2812," in *2007 9th International Conference on Electrical Power Quality and Utilisation*, IEEE, Oct. 2007, pp. 1–6, doi: 10.1109/EPQU.2007.4424233.
- [5] R. Omar and N. A. Rahim, "Modeling and simulation for voltage sags/swells mitigation using dynamic voltage restorer (DVR)," in *2008 Australasian Universities Power Engineering Conference*, 2008, pp. 1–5.
- [6] C.-S. Lam, M.-C. Wong, and Y.-D. Han, "Voltage swell and overvoltage compensation with unidirectional power flow controlled dynamic voltage restorer," *IEEE Transactions on Power Delivery*, vol. 23, no. 4, pp. 2513–2521, Oct. 2008, doi: 10.1109/TPWRD.2008.921142.
- [7] C. Benachaiba and B. Ferdi, "Voltage quality improvement using DVR," *Electrical Power Quality and Utilisation, Journal*, no. 1, p. 8, 2008.
- [8] A. M. M. Nour and A. A. Helal, "A voltage sensorless technique for a shunt active power filter adopting band pass filter under abnormal supply conditions," *Electric Power Systems Research*, vol. 238, p. 111133, Jan. 2025, doi: 10.1016/j.epsr.2024.111133.
- [9] A. Naidu, "Factors affecting patient satisfaction and healthcare quality," *International Journal of Health Care Quality Assurance*, vol. 22, no. 4, pp. 366–381, Jun. 2009, doi: 10.1108/09526860910964834.
- [10] C. Kumar and M. K. Mishra, "An improved hybrid DSTATCOM topology to compensate reactive and nonlinear loads," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 12, pp. 6517–6527, Dec. 2014, doi: 10.1109/TIE.2014.2321355.
- [11] R. Shriwastava *et al.*, "Simulation analysis of electric vehicle charging station using hybrid sources," *International Journal of Applied Power Engineering*, vol. 13, no. 1, pp. 194–200, Mar. 2024, doi: 10.11591/ijape.v13.i1.pp194-200.
- [12] R. Shriwastava, S. Gosavi, S. S. Khule, S. Hadpe, and M. P. Thakare, "A novel PWM technique for reduced switch count multilevel inverter in renewable power applications," *International Journal of Applied Power Engineering*, vol. 12, no. 1, pp. 1–12, Mar. 2023, doi: 10.11591/ijape.v12.i1.pp1-12.
- [13] S. Muthukrishnan and A. N. Kumar, "Comparison of simulation and experimental results of UPQC used for power quality improvement," *International Journal of Computer and Electrical Engineering*, vol. 2, no. 3, pp. 555–559, 2010.
- [14] R. L. V. Arnez and L. C. Zanetta, "Unified power flow controller (UPFC): its versatility in handling power flow and interaction with the network," in *IEEE/PES Transmission and Distribution Conference and Exhibition*, IEEE, 2002, pp. 1338–1343, doi: 10.1109/TDC.2002.1177674.
- [15] R. K. Pandey and N. K. Singh, "An analytical approach for control design of UPFC," in *2008 Joint International Conference on Power System Technology and IEEE Power India Conference*, IEEE, Oct. 2008, pp. 1–6, doi: 10.1109/ICPST.2008.4745186.
- [16] A. Sharma, S. K. Sharma, and B. Singh, "Unified power quality conditioner analysis design and control," in *2018 IEEE Industry Applications Society Annual Meeting (IAS)*, IEEE, Sep. 2018, pp. 1–8, doi: 10.1109/IAS.2018.8544566.
- [17] P. Kanjiya, B. Singh, A. Chandra, and K. Al-Haddad, "'SRF theory revisited' to control self-supported dynamic voltage restorer (DVR) for unbalanced and nonlinear loads," *IEEE Transactions on Industry Applications*, vol. 49, no. 5, pp. 2330–2340, Sep. 2013, doi: 10.1109/TIA.2013.2261273.
- [18] S. Kalyani and G. Das, "Simulation of DQ control system for a unified power flow controller," *ARNP Journal of Engineering and Applied Sciences*, vol. 2, no. 6, pp. 10–19, 2007, [Online]. Available: [https://www.arnpjournals.com/jeas/research\\_papers/rp\\_2007/jeas\\_1207\\_70.pdf](https://www.arnpjournals.com/jeas/research_papers/rp_2007/jeas_1207_70.pdf).

- [19] X. Y. Zhou, H. F. Wang, and R. K. Aggarwal, "Detailed modelling and simulation of UPFC using EMTP," in *39th International Universities Power Engineering Conference, 2004. UPEC 2004.*, 2004, pp. 256–260.
- [20] Z. Meng and P. L. So, "A UPFC model for dynamic stability enhancement," *IEEE Proc.*, vol. 145, no. 1, pp. 81–86, 2000.
- [21] B. Hu, K. Xie, and R. Karki, "Reliability evaluation of bulk power systems incorporating UPFC," in *2010 IEEE 11th International Conference on Probabilistic Methods Applied to Power Systems*, IEEE, Jun. 2010, pp. 259–264, doi: 10.1109/PMAPS.2010.5528714.
- [22] R. B. Gonzatti, S. C. Ferreira, C. H. Da Silva, R. R. Pereira, L. E. B. da Silva, and G. Lambert-Torres, "Smart impedance: a new way to look at hybrid filters," *IEEE Transactions on Smart Grid*, vol. 7, no. 2, pp. 837–846, Mar. 2016, doi: 10.1109/TSG.2015.2466613.
- [23] P. C. Stefanov and A. M. Stankovic, "Modeling of UPFC operation under unbalanced conditions with dynamic phasors," *IEEE Transactions on Power Systems*, vol. 17, no. 2, pp. 395–403, May 2002, doi: 10.1109/TPWRS.2002.1007909.
- [24] P. Kumkratug, "Application of UPFC to increase transient stability of inter-area power system," *Journal of Computers*, vol. 4, no. 4, pp. 283–287, 2009, doi: 10.4304/jcp.4.4.283-287.
- [25] S. Devassy and B. Singh, "Design and performance analysis of three-phase solar PV integrated UPQC," *IEEE Transactions on Industry Applications*, vol. 54, no. 1, pp. 73–81, Jan.-Feb. 2018, doi: 10.1109/TIA.2017.2754983.

## BIOGRAPHIES OF AUTHORS



**Dr. Yogesh S. Pawar**    received the B.E. degree in electrical engineering from Pune University, Nashik, PDVPCOE, Ahmednagar, Maharashtra, India, in 2010, and the M.Tech. degree in electrical power systems from Mumbai University, Veermata Jijabai Technological Institute, Mumbai, Maharashtra, India, in 2012, and his Ph.D. degree from Bhabha University, Bhopal, Maharashtra, India, in 2025. He is currently an assistant professor with the Department of Electrical Engineering, Loknete Gopinathaji Munde Institute of Engineering Education and Research, Nashik. He has over 13 years of teaching experience. His research interest includes power system, optimization techniques, and artificial intelligence techniques. He is a life member of ISTE. He can be contacted at email: [ysp.logmicer@gmail.com](mailto:ysp.logmicer@gmail.com) or [yogesh.pawar@logmicer.edu.in](mailto:yogesh.pawar@logmicer.edu.in).



**Dr. Mahesh Kadu**    completed his graduation in electronics and telecommunication engineering from Pravara Rural Engineering College (PREC) of Savitribai Phule University, India, in 2006, and M.Tech. in electronics and telecommunication engineering from Dr. BATU in 2011. He was awarded a Ph.D. by Symbiosis International University, India. His research interests are primarily in the area of wireless communications and networks. He can be contacted at email: [mahesh.kadu@gmail.com](mailto:mahesh.kadu@gmail.com).



**Dr. Pawan C. Tapre**    received the B.E. and M.E. degrees in electrical power system engineering from Sant Gadge Baba Amravati University (SGBAU), Maharashtra, India, in 1995 and 2002, respectively, and Ph.D. degree in electrical engineering from Dr. C.V. Raman University (Dr. CVRU), Bilaspur, Chhattisgarh, India, in 2022. Currently, he is an assistant professor at the Department of Electrical Engineering, S.N.D. College of Engineering and Research Center, Yeola (Nashik), Maharashtra, India. His research interests include deregulated power system, flexible AC transmission systems (FACTS), power systems, and power system protection. He can be contacted at email: [pawan.tapre73@gmail.com](mailto:pawan.tapre73@gmail.com).



**Dr. Dinesh S. Wankhede**    received the B.E. degree in electrical engineering from Amravati University, Amravati, SSGMCE, Shegaon, Maharashtra, India in 1999 and the M.E. degree in electrical power system from Shivaji University, Kolhapur, Walchand College of Engineering, Sangli, Maharashtra, India, in 2002 and his Ph.D. degree from Visvesvaraya National Institute of Technology, Nagpur, Maharashtra, India in 2019. He is currently an associate professor with the Department of Electrical Engineering, St. Vincent Pallotti College of Engineering and Technology, Nagpur. He has over 22 years of teaching experience. His research interests include power electronics, optimization techniques, and artificial intelligence techniques. He is a life member of ISTE and a recipient of the ISTE's L&T Best M.Tech. Thesis Award in 2001. He can be contacted at email: [dineshhwankhede@gmail.com](mailto:dineshhwankhede@gmail.com) or [dwankhede@stvincentngp.edu.in](mailto:dwankhede@stvincentngp.edu.in).



**Dr. Rajendra M. Rewatkar**    obtained his B.E. degree in electronics engineering from RTM Nagpur University, Nagpur, India, in 1996. He received the M.Tech. degree in electronics engineering from G.H. Rasoni College of Engineering, Nagpur, India, in 2010. He has been awarded a doctoral degree in electronics engineering from RTM Nagpur University, Nagpur (India) in 2016. He occupied various positions to serve the Engineering Institutes for about 27 years. He is currently working as an associate professor and head of Biomedical Engineering Department of the Faculty of Engineering and Technology, Datta Meghe Institute of Higher Education and Research, Sawangi (Meghe), Wardha. His research interests include signal processing and CMOS VLSI design. He is a fellow of IETE and a life member of the professional bodies such as ISTE, IE, and IAENG. He can be contacted at email: [rajendrarr.feat@dmier.edu.in](mailto:rajendrarr.feat@dmier.edu.in).



**Dr. Swapna M. Choudhary**    is currently working as an assistant professor in electronics and telecommunications engineering at GH Rasoni College of Engineering, Nagpur. She has done her graduation in electronics engineering, post-graduation in VLSI, and Ph.D. in electronics engineering from RTM, Nagpur University, Nagpur. She is a recipient of prestigious Lilawati Award by AICTE, Delhi. Her research areas are VANET, machine learning, and internet of things electronics communication. She has published several papers in reputed international conferences and journals. Her research interests include signal processing and CMOS VLSI design. She has several publications in national and international journals. She attended international and national conferences. She can be contacted at email: [swapna2k11@gmail.com](mailto:swapna2k11@gmail.com).



**Dr. Rakesh G. Shriwastava**    obtained Ph.D. degree in electrical engineering, specializing in power electronics and drives from RTM Nagpur University (India) in 2017. He occupied various positions to serve the engineering institutes for about 24 years. He is currently working as a professor in the Department of Electrical Engineering, Govindrao Wanjari College of Engineering and Technology, Nagpur. His research interests include the analysis and control of electrical drives, particularly in hybrid and electric vehicle applications. He has several publications in national and international journals. He attended international and national conferences and also worked as a jury member. He is a member of professional bodies such as ISTE and IAENG. He can be contacted at email: [rakesh\\_shriwastava@rediffmail.com](mailto:rakesh_shriwastava@rediffmail.com).